Patent Claims

1. An electronic transmitter device having a puncturing device, wherein the puncturing device

- has a first and a second data output,
- is configured in such a way that it distributes its output data stream essentially uniformly in parallel between its said two data outputs,
- provides empty locations in its output data stream so that the number of bits of the input data stream corresponds, including the empty locations, to the number of bits of the output data stream, and
- outputs in addition to its parallel output data stream, a signal which indicates to the puncturing device empty locations in the parallel output data stream.

2. An electronic transmitter device having an interleaver (2), characterized in that the interleaver (2) has two data inputs and is configured in such a way that it can process data streams coming in in parallel at both data inputs.

3. The electronic transmitter device as claimed in claim 2, characterized in that the interleaver (2) is a block interleaver which has parallel data inputs.

4. The electronic transmitter device as claimed in claim 1, characterized in that it has an interleaver (2) which is arranged downstream of the puncturing device in the direction of the data stream and which

- has a first data input which is directly or indirectly electrically connected to the first data output of the puncturing device, and

- a second data input which is directly or indirectly electrically connected to the second data output of the puncturing device.

5. The electronic transmitter device as claimed in one of claims 2 to 4, characterized in that the interleaver (2) is an n × m interleaver, n and m being natural numbers.

6. The electronic transmitter device as claimed in one of claims 2 to 5, characterized in that the interleaver (2) has a first shift register which is directly or indirectly electrically connected to its first data input, and a second shift register which is directly or indirectly electrically connected to its second data input.

7. The electronic transmitter device as claimed in claim 6 which is referred back to claim 5, characterized in that both shift registers are -bit shift registers.

8. The electronic transmitter device as claimed in claim 6 or 7, characterized in that the interleaver (2) has a matrix register.

9. The electronic transmitter device as claimed in claim 8, characterized in that the matrix register is a 16 × 18 matrix register.

10. The electronic transmitter device as claimed in claim 8 or 9, characterized in that in each case two bits are written in parallel into the matrix register from the two shift registers.

11. The electronic transmitter device as claimed in claim 8 or 9, characterized in that after the two shift

registers have been completely filled by inputs via the corresponding data inputs of the interleaver (2), their bits are input together as a bit column into the matrix register, interleaved in the manner of a comb, and in this way they gradually fill up a plurality of, or all of, the columns of the matrix register.

12. The electronic transmitter device as claimed in one of claims 2 to 5, characterized in that the interleaver (2) has an RAM and is designed in such a way that the bit pairs which pass into the interleaver (2) are written directly to predetermined RAM addresses.

13. The electronic transmitter device as claimed in claim 4, characterized in that

- the interleaver (2) is configured in such a way that, using the said signal (data_valid) which is additionally transmitted by the puncturing device, it detects the empty locations in the parallel input data stream coming from the puncturing device, and does not include them in the further data processing.

14. The electronic transmitter device as claimed in claim 1, characterized in that the puncturing device is composed of precisely one puncturing element (P2).

15. The electronic transmitter device as claimed in claim 1, characterized in that the puncturing device has a first puncturing element (P1) and a second puncturing element (P2) which is arranged downstream of the first puncturing element (P1) in the direction of the data stream.

16. The electronic transmitter device as claimed in claim 15, characterized in that

- the first puncturing element (P1) has a first and

a second data output and is configured in such a way that it

distributes its output data stream essentially uniformly between its two data outputs, and

- the second puncturing element (P2) has a first and a second data input, the first data input of the second puncturing element (P2) being directly or indirectly electrically connected to the first data output of the first puncturing element (P1), and the second data input of the second puncturing element (P2) being directly or indirectly electrically connected to the first data output of the first puncturing element (P1).

17. The electronic transmitter device as claimed in claim 16, characterized in that

- the first puncturing element (P1) is configured in such a way that, in addition to its parallel output data stream, it transmits to the second puncturing element (P2) a signal (data_valid) which informs the second puncturing element (P2) about empty locations in the parallel output data stream of the first puncturing element (P1), and
- the second puncturing element (P2) is configured in such a way that, using the said signal (data_valid) which is additionally transmitted by the first puncturing element (P1), it detects the empty locations in the parallel input data stream coming from the first puncturing element (P1), and does not include them in the further data processing.

18. The electronic transmitter device as claimed in claim 16 or claim 17, characterized in that the first puncturing element (P1) has a first data input (IN_X) and a second data input (IN_Y), and is configured in such a way that

- a 1-step delay register (D) is connected between the first data input (IN_X) and the first data output (Out_X),

- the second data input (IN_Y) is electrically connected to a first input of a multiplexer (MUX) via a 1-step delay register (D), and in parallel with this

it is directly electrically connected to a second input of a multiplexer (MUX), and

- the multiplexer (MUX) has an output which is electrically connected to the second data output (Out_Y) of the first puncturing element (P1) via a further 1-step delay register (D).

19. The electronic transmitter device as claimed in one of claims 15 to 18, characterized in that the second puncturing element (P2) has two data outputs.

20. The electronic transmitter device as claimed in claim 19, characterized in that the two data outputs of the second puncturing element (P2) are simultaneously the two data outputs of the puncturing device.

21. The electronic transmitter device as claimed in claim 19 or claim 20, characterized in that

- the second puncturing element (P2) has three multiplexers (MUX) which each have two inputs and one output,
- the first data input (IN_X) of the second puncturing element (P2) is directly electrically connected both to the first input of the first multiplexer of the second puncturing element (P2) and to the first input of the second multiplexer of the second puncturing element (P2),
- the second data input (IN_Y) of the second puncturing element (P2) is directly electrically connected both to the second input of the first multiplexer of the second puncturing element (P2) and to the second input of the second multiplexer of the second puncturing element (P2),
- the output of the first multiplexer of the second puncturing element (P2) is directly electrically connected to the first input of the third multiplexer of the second puncturing element (P2),

- the output of the first multiplexer of the second puncturing element (P2) is electrically connected via a 1-step delay register (D) to the second input of the third multiplexer of the second puncturing element (P2),
- the output of the third multiplexer of the second puncturing element (P2) is electrically connected via a 1-step delay register (D) to the first data output (Out_X) of the second puncturing element (P2), and
- the output of the second multiplexer of the second puncturing element (P2) is electrically connected via a further 1-step delay register (D) to the second data output (Out_Y) of the second puncturing element (P2).

22. An electronic receiver device having a de-interleaver (3) which has a first data output, characterized in that the de-interleaver (3)

- has a second data output, and
- is configured in such a way that it distributes its output data stream essentially uniformly in parallel between its said two data outputs.

23. The electronic receiver device as claimed in claim 22, characterized in that the de-interleaver (3) is an n × m de-interleaver, n and m being natural numbers.

24. The electronic receiver device as claimed in claim 22 or claim 23, characterized in that the de-interleaver (3) has a matrix register.

25. The electronic receiver device as claimed in claim 24, characterized in that the matrix register is a 16 × (18 × N) matrix register, N being the word length of the soft bits.

26. The electronic receiver device as claimed in claim 24 or 25, characterized in that the de-interleaver (3) is configured in such a way that in each case two soft bits are read out in parallel from the matrix register.

27. The electronic receiver device as claimed in one of claims 23 to 26, characterized in that the de-interleaver (3) has a first shift register which is directly or indirectly electrically connected to its first data output, and a second shift register which is directly or indirectly electrically connected to its second data output, the two said shift registers being configured as soft bit shift registers.

28. The electronic receiver device as claimed in claim 27 which is referred back to claim 23, characterized in that both shift registers are soft bit shift registers.

29. The electronic receiver device as claimed in claim 27 or 28, characterized in that the de-interleaver (3) is configured in such a way that, when the data is output from the n × m structure or from the matrix register, at first a column is output interleaved in the manner of a comb, i.e. is output to the two shift registers in such a way that two adjacent soft bits are respectively fed to a different shift register, and then both shift registers are read out simultaneously, and after the reading out of the two shift registers further data columns are successively output to the two shift registers from the n × m structure or from the matrix register in the same way as with the first column which is output.

30. The electronic receiver device as claimed in claim 22, characterized in that the de-interleaver (3) has an RAM and is configured in such a way that when data is output the bit pairs from the RAM are fed directly to the two data outputs of the de-interleaver (3).

31. An electronic receiver device having
- a de-interleaver (3) and
- a depuncturing device which is arranged downstream of the de-interleaver (3) in the direction of the data stream,

the de-interleaver (3)
- having a first and a second data output,
- being configured in such a way that it distributes its output data stream essentially uniformly in parallel between its said two data outputs,
- provides empty locations in its output data stream so that the number of bits of the output data stream of the de-interleaver (3) corresponds, including the empty locations, to the number of bits of the output data stream of the depuncturing device, and
- transmits, in addition to its parallel output data stream, to the depuncturing device a signal (data_valid) which informs the depuncturing device about empty locations in the parallel output data stream of the de-interleaver (3).

32. The electronic receiver device as claimed in claim 31, characterized in that the depuncturing device which is arranged downstream of the de-interleaver (3) in the direction of the data stream has two data inputs, the first data input of the depuncturing device being directly or indirectly electrically connected to the first data output of the de-interleaver (3), and the second data input of the depuncturing device being directly or indirectly electrically connected to the second data output of the de-interleaver (3).

33. The electronic receiver device as claimed in claim 32, characterized in that
- the depuncturing device is configured in such a way that, using the said signal (data_valid) which

is additionally transmitted by the de-interleaver (3), it detects the empty locations in the parallel input data stream coming from the de-interleaver (3) and fills them with soft zeros during the further data processing.

34. An electronic receiver device having a depuncturing device, the depuncturing device having two data inputs and being configured in such a way that it can process data streams coming in in parallel at both data inputs, and has a first depuncturing element (P2') and a second depuncturing element (P1') which is arranged downstream of the first depuncturing element (P2') in the direction of the data stream,

- the first depuncturing element (P2') providing empty locations in its output data stream so that the number of bits of the output data stream of the first depuncturing element (P2') corresponds, including the empty locations, to the number of bits of the output data stream of the second depuncturing element (P1'), and
- the first depuncturing element (P2') is configured in such a way that, in addition to its parallel output data stream, it transmits to the second depuncturing element (P1') a signal (data_valid) which informs the second depuncturing element (P1') about empty locations in the parallel output data stream of the first depuncturing element (P2').

35. The electronic receiver device as claimed in claim 34, characterized in that the first depuncturing element (P2') has

- a first multiplexer (MUX) having two inputs and one output,
- a second multiplexer (MUX) having two inputs and one output, and

- a third multiplexer (MUX) having four inputs and one output, in each case a 1-step delay register (D) is connected between
- the output of the first multiplexer (MUX) and one input of the second multiplexer (MUX),

- the output of the second multiplexer (MUX) and a first data output (Out_X) of the first depuncturing element (P2'),
- the output of the third multiplexer (MUX) and a second data output (Out_Y) of the first depuncturing element (P2'), and
- a first data input (IN_Y) of the first depuncturing element (P2') and an input of the third multiplexer (MUX),

and

- the first data input (IN_Y) of the first depuncturing element (P2') is also directly electrically connected to an input of the first multiplexer (MUX) and to a further input of the third multiplexer (MUX),
- the second data input (IN_X) of the first depuncturing element (P2') is directly electrically connected to the further input of the second multiplexer (MUX), and the third input of the third multiplexer (MUX), and
- the respectively remaining input of the first multiplexer (MUX) and of the third multiplexer (MUX) is connected to a line on which soft zeros are made available.

36. The electronic receiver device as claimed in claim 34 or claim 35, characterized in that the second depuncturing element (P1') has three multiplexers (MUX) each with two inputs and one output, in each case a 1-step delay register (D) is connected between

- the output of the first multiplexer (MUX) and an input of the second multiplexer (MUX),
- the output of the second multiplexer (MUX) and the first data output (Out_X) of the second depuncturing element (P1'), and

- the output of the third multiplexer (MUX) and the second data output (Out_Y) of the second depuncturing element (P1'), and
- the first data input (IN_X) of the second depuncturing element (P1') is directly electrically connected to an input of the first multiplexer (MUX) and to the further input of the second multiplexer (MUX),
- the second data input (IN_Y) of the second depuncturing element (P1') is directly electrically connected to an input of the third multiplexer (MUX), and
- the respectively remaining input of the first multiplexer and of the third multiplexer (MUX) is connected to a line on which soft zeros are made available.

37. The electronic receiver device as claimed in one of claims 34 to 36, characterized in that

- the first depuncturing element (P2') has a first and a second data output and is configured in such a way that it distributes its output data stream essentially uniformly between its two data outputs, and
- the second depuncturing element (P1') has a first and a second data input, the first data input of the second depuncturing element (P1') being directly or indirectly electrically connected to the first data output of the first depuncturing element (P2'), and the second data input of the second depuncturing element (P1') is directly or indirectly electrically connected to the first data output of the first depuncturing element (P2').

38. The electronic receiver device as claimed in one of claims 34 to 37, characterized in that

- the second depuncturing element (P1') is configured in such a way that, using the said signal (data_valid) which is additionally transmitted by the first depuncturing element (P2'), it detects the empty locations in the parallel input data stream coming from the first depuncturing element (P2') and fills them with soft zeros during the further data processing.

39. The electronic receiver device as claimed in one of claims 34 to 38, characterized in that the first depuncturing element (P2') has two data inputs.

40. The electronic receiver device as claimed in claim 39, characterized in that the two data inputs of the first depuncturing element (P2') are simultaneously the two data inputs of the depuncturing device.

41. A telecommunications transmission system, characterized in that it has an electronic transmitter device as claimed in one of claims 1 to 21 and/or an electronic receiver device as claimed in one of claims 22 to 40.

42. The telecommunications transmission system as claimed in claim 41, characterized in that it is configured in such a way that the transmission between the transmitter and receiver is carried out in a wirefree fashion.

43. The telecommunications transmission system as claimed in claim 42, characterized in that it is a WLAN.

44. The telecommunications transmission system as claimed in one of claims 41 to 43, characterized in that the clock frequency of the system is in the region between 75 MHz and 85 MHz.

45. The telecommunications transmission system as claimed in claim 44, characterized in that the clock frequency of the system is 80 MHz.